We claim:

1. A carry-save adder for adding bits of the same weight, comprising:
   - six inputs for receiving six bits of in each case the same weight w, which are to be added,
   - one output for a sum bit of the weight w and two outputs for two carry bits of the weights 2w and 4w, and
   - three adder subblocks which are arranged in parallel with one another and are not interconnected, wherein the first adder subblock generates the sum bit, the second adder subblock generates the carry bit of weight 2w and the third adder subblock generates the carry bit of weight 4w, each adder subblock being built up from logic gates.

2. The carry-save adder as claimed in claim 1, wherein
   - a and in particular each adder subblock is implemented from a maximum of three series-connected logic gate stages.

3. The carry-save adder as claimed in claim 2, wherein
   - the first adder subblock comprises in the first stage three XOR gates, in the second stage one XOR gates receiving input signals from the first two XOR gates of the first stage and in the third stage one XOR gate which receiving input signals from the XOR gate of the second stage and from the third XOR gate of the first stage.

4. The carry-save adder as claimed in claim 2, wherein
   - the second and third adder subblock each comprise in the first stage a plurality of NAND gates generating a plurality of output signals, in the second stage a plurality of AND gates combining the signals from the first stage generating three output signals and in the third stage one NAND gate combining the three signals from the second stage.

5. The carry-save adder for adding bits of the same weight, comprising:
   - six inputs for receiving six bits of in each case the same weight w, which are to be added,
   - one output for a sum bit of the weight w and two outputs for two carry bits of weight 2w and 4w, and
   - three adder subblocks connected in parallel with one another and not interconnected, wherein the first adder subblock generates the sum bit, the second adder subblock generates the carry bit of weight 2w and the third adder subblock generates the carry bit of weight 4w, and each adder subblock consists of a multitransistor circuit which cannot be resolved into logic gates,
   - wherein in the multitransistor circuit which forms the adder subblock for calculating the sum bit, one input drives two and the remaining inputs drive four transistors.

6. The carry-save adder as claimed in claim 5, wherein
   - in the multitransistor circuit which forms the adder subblock for calculating the carry bit of weight 2w, a first input drives two transistors, a second and a third input in each case drive four transistors, a fourth input drives six transistors and a fifth and a sixth input in each case drive eight transistors.

7. The carry-save adder as claimed in claim 6, wherein
   - in the multitransistor circuit which forms the adder subblock for calculating the carry bit of weight 4w, a first and a second input in each case drive two transistors, a third and a fourth input in each case drive four transistors and a fifth and a sixth input in each case drive six transistors.

8. The carry-save adder as claimed in claim 5, comprising:
   - a charging circuit which is connected to the multitransistor circuit, in such a manner that it is discharged via the latter in dependence on the bits present at the inputs of the adder.